UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/334,530	06/16/1999	KORBIN S. VAN DYKE	30585/10	5424

7590 12/30/2002

DAVID E BOUNDY
SCHULTE ROTH & ZABEL
919 THIRD AVENUE
NEW YORK, NY 10022

EXAMINER
DAS, CHAMELI

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/334,530	Applicant(s) VAN DYKE ET AL.	
	Examiner C..DAS	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37 and 41-45* is/are rejected.

7)☒ Claim(s) *38-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-45 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-9, 13-37 and 41-43 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Donnell, US 6,374,369.

As per claim 1, O'Donnell discloses:

- while executing a program on a computer, detecting the occurrence of profileable events (Abstract, lines 1-16, column 4, lines 21-25)

- ***occurring in the instruction pipeline*** (column 11, lines 38-40), the execution of the program is sequential and the observer executes concurrently inherently including instruction pipeline as claimed

- ***directing the instruction pipeline to record profile information describing the profileable events essentially concurrently with the occurrence of the profileable events*** (column 5, lines 19-22, column 6, lines 46-52, abstract lines 1-16).

O'Donnell discloses detecting and recording occurring under control of hardware of the computer without software intervention (column 1, lines 8-12, Abstract lines 4-16, column 9, lines 38-40, column 7, lines 38-42, column 8, lines 1-4), where performance measure using in response to one of a hardware interrupt and hardware being used during the execution of the profiling process inherently including recording occurring under control of hardware without software intervention as claimed.

As per claim 2, O'Donnell discloses:

- ***recorded profileable events indicates the address as claimed*** (column 15, lines 17-62), where "profile starts" and "profile stop" shows that profiled execution interval as claimed.

As per claim 3, 25, O'Donnell discloses:

- ***one of the recorded profileable events notes the source and destination of a control flow event in which control flow of the program execution diverges from sequential execution*** (column 3, lines 45-57), where finite state of automation includes the source and destination of

control flow (column 5, lines 23-33) and executing the application software and the finite state automation in an interleaved fashion inherently including execution diverges from sequential execution as claimed.

As per claim 4, 26, O'Donnell discloses:

- executing the program on a first CPU (column 4, lines 29-30), where second device for executing is the first CPU

- second CPU of the multi processor , while the execution and profiling of the program continues (column 4, lines 26-29), where first device for executing is the second CPU of the multi processor

- controlling the execution of the program as claimed (column 4 lines 23-37).

As per claim 5, 27, O'Donnell discloses:

- the profile information is recorded into general registers of the computer under hardware control, without software intervention (Abstract lines 4-8, column 2 lines 63-67 and column 3 lines 1-5 and column 16 lines 22-27)

- without first storing the profile information into main memory (column 6, lines 53-55).

As per claim 6, 42, O'Donnell discloses:

- TLB mis and reflecting the corrected state as claimed (column 10, lines 48-63, and column 11 lines 18).

As per claim 7, O'Donnell discloses:

- a triggering event is detected, the triggering event being one of pre-defined class of triggering events, continuing the execution of the program and recording profile entries in a memory as claimed (Abstract lines 1-16, column 6 lines 15-31).

As per claim 8, O'Donnell discloses:

- recording profile information that records a sequence of events of the program as claimed (column 6 lines 1-37) triggering events that matches time-independent criteria is shown in column 8 lines 54-57.

As per claim 9, 20 O'Donnell discloses:

- triggering event is expiration of a timer (column 9 lines 65-67 and column 10 lines 1-19).

As per claim 13, O'Donnell discloses:

- recording in a processor mode that determines the meaning of the instruction (column 10, lines 42-46), the instructions are binary is shown in (column 30-32).

As per claim 14, O'Donnell discloses:

- recording profile information recording a data-dependent change (Abstract 1-16, column 11 lines 1-11), fully/empty mask for registers is shown in column 10 lines 35-37.

As per claim 15, 28, O'Donnell discloses:

- recorded profile information being efficiently tailored to identify all bytes of object code executed during the profiled execution interval as claimed (Abstract, lines 1-16 and column 4 lines 38-58.

As per claim 16, 29, O'Donnell discloses:

- recording profile information that records a sequence of events of the program as claimed (column 6 lines 45-53), time independent criteria is shown in column 8 lines 54-57.

As per claim 17, 30, O'Donnell discloses:

- recorded profile information indicates ranges as claimed (column 10 lines 26-40).

As per claim 18, O'Donnell discloses:

- subunits of two kinds, a first suubunit kind describing an instruction interpretation mode as claimed (column 7 lines 1-4), where compiles the profiling software is the instruction interpretation as claimed

- second subunit kind describing a transition between processor modes (column 4, lines 35), where first, second, third processors are using inherently including describing a transition between processor modes as claimed.

As per claim 19, 31, O'Donnell discloses:

- program execution induces occurrence of events that match time independent criteria as claimed is shown in (Abstract lines 1-16, column 8, lines 54-59)

- during profile-quiescent interval of execution, recording no profile information as claimed (Abstract, lines 1-16 and column 5, lines 50-52), where stop profiles means recording no profile information as claimed

- initiating the profiled execution as claimed (column 8, lines 28-54)

As per claim 21, O'Donnell discloses:

- prolileable events divide the prolileable events into initialing and non-initiating events and describing every initiating and non-initiating events as claimed (Abstract, lines 1-16, column 5, lines 25-26, column 5, lines 36-37), where trigger events are describing initiating events and terminate trigger phase in the finite state automaton describes non-initialing events.

As per claim 22, O'Donnell discloses:

recording a time stamp of the events as claimed (Abstract, lines 5-8), timer is used for record timining inherently including time stamp describing time of the recorded events.

As per claim 23, O'Donnell discloses:

- instruction pipeline as claimed (column 6, lines 45-60).

As per claim 24, O'Donnell discloses:

- computer hardware comprising an instruction pipeline (Abstract, lines 1-16, column 6, lines 45-60)

- an arithmetic unit (Fig 9), where "510" and "530" show the loop counting and timer count inherently including an arithmetic unit is the hardware system as claimed

- execute instructions received from a memory and profile circuitry (Abstract, lines 3-12, column 4, lines 38-44)

- profile circuitry under hardware control, the instruction pipeline interconnected to detect

- detecting and recording occurring under control of hardware of the computer without software intervention (column 1, lines 8-12, Abstract lines 4-16, column 9, lines 38-40, column 7, lines 38-42, column 8, lines 1-4), where performance measure using in response to one of a hardware interrupt and hardware being used during the execution of the profiling process inherently including recording occurring under control of hardware without software intervention as claimed.

As per claim 32, O'Donnell discloses:

- a register pointer being a register of the computer indicating a general register into which to record profile as claimed (column 10, lines 27-40)

- an increment configured to increment the value of the register as claimed (column 12 lines 66-67 and column 13 lines 1-27).

As per claim 33, O'Donnell discloses:

- a limit detector operatively interconnected with the register pointer to detect when a range of registers available for collecting profile as claimed (column 10, lines 27-40), where represented by two registers specifying a range of addresses inherently including a limit detector as claimed, profile information is exhausted is shown in column 5, lines 50-52, storing the profile into the memory (column 6, lines 10-25, column 10, lines 21-26).

As per claim 34, O'Donnell discloses:

- profile control bits implemented in the computer hardware as claimed (column 10, lines 35-37)

- binary translator configured to translate programs coded as claimed (column 6 line 65-67 and column 7 lines 1-16), where data interpretation program is the translator to translate programs, the software is in binary format (column 15 lines 30-32) shows that the translator is the binary translator as claimed.

- the profile circuitry is interconnected with the instruction pipeline and store in the register (column 5, line 66-67 and column 6 lines 1-60 and column 10 lines 31-40).

As per claim 35, O'Donnell discloses:

- profile circuitry is interconnected with the instruction pipeline to direct recording as claimed (Abstract lines 1-16, column 3 lines 44-52, column 6 lines 45-60, column 10, lines 27-40).

As per claim 36 O'Donnell discloses:

- instruction pipeline and profile circuitry are operatively interconnected (column 5, lined 66-67 and column 6 lines 1-9, column 9 lines 40-45).

As per claim 37, O'Donnell discloses:

pipeline and profile circuitry are operative interconnected as claimed (column 9, lines 40-45, column 11 lines 22-8).

As per claim 41, O'Donnell discloses:

- profile circuitry comprises a plurality of storage registers as claimed (column 10, lines 27-40, column 6, lines 40-52, Abstract lines 1-5).

As per claim 42, O'Donnell discloses:

- when an instruction fetch of an instruction causes a miss in translation look aside buffer (TLB) as claimed (column 10 lines 63- 67, column 11 line 17- 27).

As per claim 43, O'Donnell discloses:

- timer interval value as claimed (column 9, lines 36-64, column 14, line 19 and column 14, lines 33-37).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-12, rejected under 35 U.S.C. 103(a) as being unpatentable over O'Donnell (US 6,374,369) above, and further in view of Ju et al (US 6,175,957)

As per claim 10, O'Donnell discloses:

- recorded physical memory references include address of instructions referenced by an instruction pointer (column 7 lines 1-9, column 12 lines 50-55, column 15 lines 18-21), the

instructions are binary is shown in (column 15, lines 25-30), records the event of a sequential execution flow is shown in (abstract, lines 1-16 and column 6 lines 53-60).

O'Donnell does not specifically disclose page boundary. However, Ju discloses the page boundary (column 2, lines 40-41).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to incorporate the teaching of Ju into the method of O'Donnell for having page boundary. The modification would be obvious because one of the ordinary skill in the art would want to reduce communications between the instructions.

As per claim 11 O'Donnell discloses:

- events occurring within a single instruction (column 11, lines 19-21 and column 10 lines 41-45), for page boundary see the rejection of claim 10.

As per claim 12 O'Donnell discloses:

- event occurs between two instructions that are sequentially adjacent (column 6, lines 46-51, column 6 lines 58-60), in the logical address space is shown in column 10 lines 27-28, for page boundary see the rejection of claim 10.

5. Claims 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Donnell (US 6,374,369) further in view of Agesen et al (US 6,253,215)

As per claim 44, O'Donnell doest not specifically disclose two substantially disjoint instructions, a native instruction set providing access to substantially all of the resources of the

computer and a non-native instruction sets providing access to a subset of the resources of the computer. However, Agesen discloses two substantially disjoint instructions, a native instruction set providing access to substantially all of the resources of the computer and a non-native instruction sets providing access to a subset of the resources of the computer (abstract lines 1-17, column 1, lines 9-15, column 5 lines 1-15).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to incorporate the teaching of Agesen into the method of O'Donnell for having two types of instructions and providing all of the resources to the native instructions and subset of resources to the non-native instructions . The modification would be obvious because one of the ordinary skill in the art would want to manage the resources of the computer systems between the instructions efficiently.

As per claim 45, O'Donnell discloses recording the profile information an interval of the execution as claimed (Abstract lines 1-16, column 4 lines 1-44).

As per claim 45, O'Donnell doest not specifically disclose that the code is non-native instruction set. However, Agesen discloses the non-native instruction sets (column 1 lines 13-16), where target code is the non-native instructions (column 2, lines 36-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention was made to incorporate the teaching of Agesen into the method of O'Donnell for having non-native instruction. The modification would be obvious because one of the ordinary skill in the art would want to have the flexible approach for garbage collection associated with

the execution of systems having both native and target code (non-native code) (column 6 lines 23-26).

Allowable Subject Matter

6. Claims 38-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The cited prior art taken alone or in combination fail to teach a method for having a primary effect on the execution the computer not related to profiling, has as immediate field for an event code encoding the nature of profiled event and to be recorded in the profile information, the immediate field having no effect on computer execution other than to determined the event code of the profiled event as recited on the claim 38.

Conclusion

7. The prior art made or record and not relied upon is considered pertinent to applicant's disclosure.

TITLE: Method and apparatus for data flow analysis, US 6226789 B1

TITLE: Method and apparatus for multi platform stateless instruction set architecture (ISA) using ISA tags on-the-fly instruction translation, US 6496922 B1

TITLE: Low overhead speculative selection of hot traces in a caching dynamic translator, US 6470492 B2

TITLE: System and method employing buffering mechanism with interface for providing compatibility between recording formats, US 5774287 A

TITLE: Automated processor generation system for designing a configurable processor and method for the same, US 6477683 B1

TITLE: Apparatus for and method of automatic monitoring of computer performance, US 6405327 B1

TITLE: Relation-based ordering of objects in an object heap, US 6480862 B1

TITLE: System and method for controlling an instrumentation system, US 5847955 A

TITLE: Split embedded DRAM processor, US 6026478 A

TITLE: High frequency sampling of processor performance counters, US 5796939 A

TITLE: A performability model for soft real-time systems, author: Hee Yong Youn; Hurson, A.R.; Kavi, K.M.; Shirazi, B. System Sciences, 1994. Vol.II: Software Technology, Proceedings of the Twenty-Seventh Hawaii International Conference on , 4-7 Jan 1994, Source: IEEE.

TITLE: Commercializing profile-driven optimization Conte, T.M.; Cox, J.S.; Howell, D.P.; System Sciences, 1995. Vol. II. Proceedings of the Twenty-Eighth, Hawaii International Conference on , 3-6 Jan 1995, Source: IEEE

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chameli Das whose telephone number is 703-306-3014.

The examiner can normally be reached on Monday-Friday from 8:00 .A.M to 4:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Greg Morse can be reached at 703-308-4789. The fax number for this group are:

(703) 746-7239 (official fax), (703) 746-7240 (non-official/draft), (703)746-7238 (after final).

An inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is 703-305-9600.

Chameli C Das

Chameli C. Das

Patent Examiner

Art Unit 2122

12/27/02

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in ABANDONMENT of the application